

**HIGH CURRENT PHASE CONTROL  
THYRISTOR INSULATED MODULE**

# AZT460

Repetitive voltage up to **4500 V**  
Mean forward current **472 A**  
Surge current **11 kA**

**FINAL SPECIFICATION**

Feb. 18 - Issue: 4

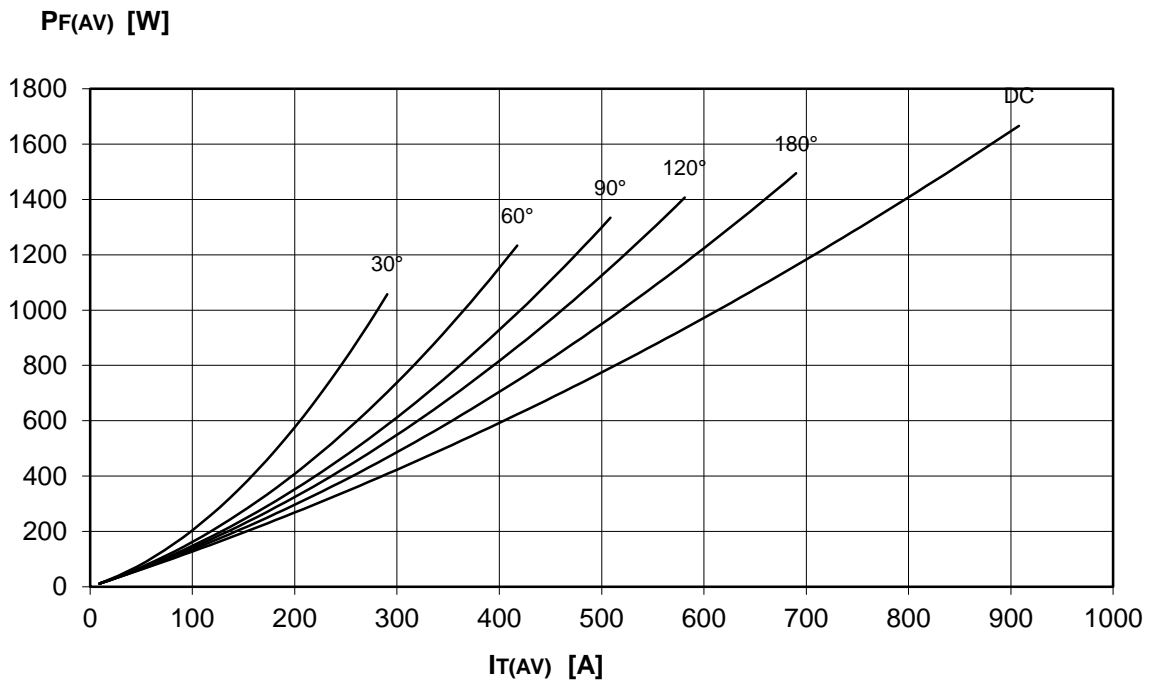
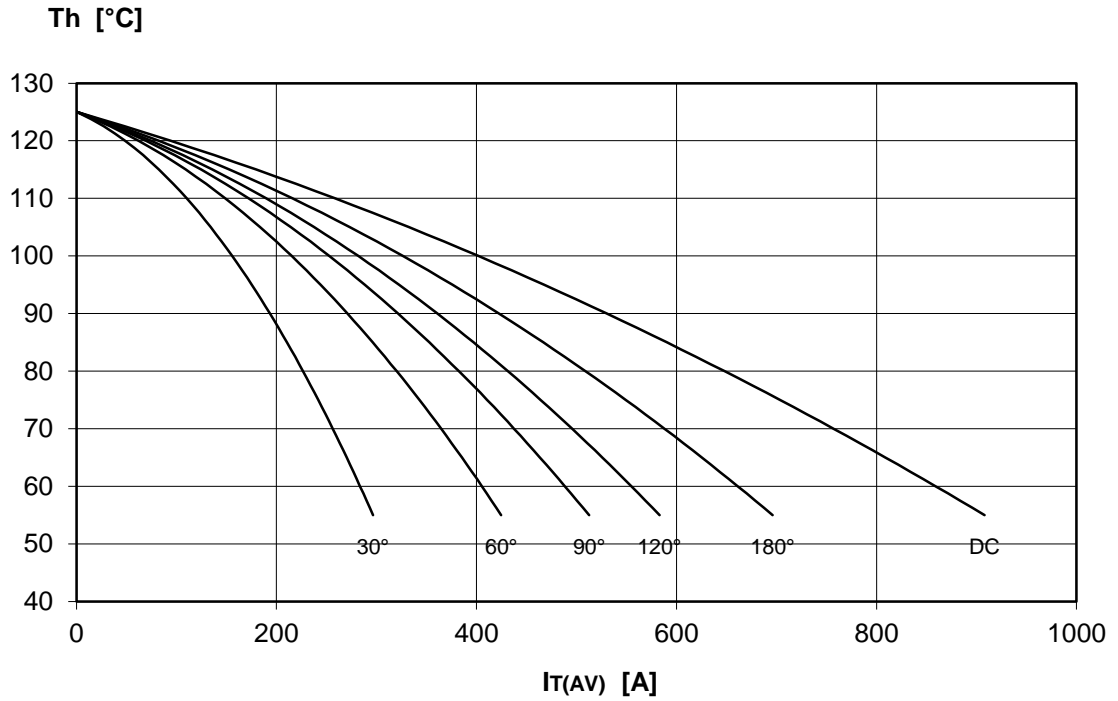
Symbol	Characteristic	Conditions	T <sub>j</sub> [°C]	Value	Unit
<b>BLOCKING</b>					
V <sub>RRM</sub>	Repetitive peak reverse voltage		125	4500	V
V <sub>RSM</sub>	Non-repetitive peak reverse voltage		125	4600	V
V <sub>DRM</sub>	Repetitive peak off-state voltage		125	4500	V
I <sub>RRM</sub>	Repetitive peak reverse current		125	100	mA
I <sub>DRM</sub>	Repetitive peak off-state current		125	100	mA
<b>CONDUCTING</b>					
I <sub>T(AV)</sub>	Mean forward current	180° sin, 50 Hz, T <sub>c</sub> =55°C, double side cooled		695	A
I <sub>T(AV)</sub>	Mean forward current	180° sin, 50 Hz, T <sub>c</sub> =85°C, double side cooled		472	A
I <sub>TSM</sub>	Surge forward current	Sine wave, 10 ms	125	11	kA
I <sup>2</sup> t	I <sup>2</sup> t	without reverse voltage		605 x 10 <sup>3</sup>	A <sup>2</sup> s
V <sub>T</sub>	On-state voltage	On-state current = 1800 A	25	2,66	V
V <sub>T(TO)</sub>	Threshold voltage		125	1,20	V
r <sub>T</sub>	On-state slope resistance		125	0,700	mohm
<b>SWITCHING</b>					
di/dt	Critical rate of rise of on-state current, min.	From 75% V <sub>DRM</sub> up to 1050 A; gate 10V, 5Ω	125	400	A/μs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of V <sub>DRM</sub>	125	1000	V/μs
t <sub>d</sub>	Gate controlled delay time, typical	VD=100V; gate source 25V, 10Ω, tr=.5 μs	25	3	μs
t <sub>q</sub>	Circuit commutated turn-off time, typical	dv/dt = 20 V/μs linear up to 75% V <sub>DRM</sub>		350	μs
Q <sub>rr</sub>	Reverse recovery charge	di/dt = -20 A/μs, I <sub>r</sub> = 700 A	125		μC
I <sub>rr</sub>	Peak reverse recovery current	VR= 50 V			A
I <sub>H</sub>	Holding current, typical	VD=5V, gate open circuit	25		mA
I <sub>L</sub>	Latching current, typical	VD=5V, tp=30μs	25		mA
<b>GATE</b>					
V <sub>GT</sub>	Gate trigger voltage	VD=5V	25	3,50	V
I <sub>GT</sub>	Gate trigger current	VD=5V	25	300	mA
V <sub>GD</sub>	Non-trigger gate voltage, min.	VD=V <sub>DRM</sub>	125	0,25	V
V <sub>FGM</sub>	Peak gate voltage (forward)			30	V
I <sub>FGM</sub>	Peak gate current			10	A
V <sub>RGM</sub>	Peak gate voltage (reverse)			5	V
P <sub>GM</sub>	Peak gate power dissipation	Pulse width 100 μs		150	W
P <sub>G</sub>	Average gate power dissipation			2	W
<b>MOUNTING</b>					
R <sub>th(j-c)</sub>	Thermal impedance, DC	Junction to case, per element		42,0	°C/kW
R <sub>th(c-h)</sub>	Thermal impedance	Case to heatsink, per element		20	°C/kW
T <sub>j</sub>	Operating junction temperature			-30 / 125	°C
V <sub>ins</sub>	RMS insulation voltage	50 hz, circuit to base, all terminal shorted	25	4500	V
T	Mounting torque	Case to heatsink		4,0 / 6,0	kN
		Busbars to terminals		12,0 / 18,0	kN
	Mass			2800	g

**ORDERING INFORMATION : AZT460 S 45**

standard specification   VRRM/100

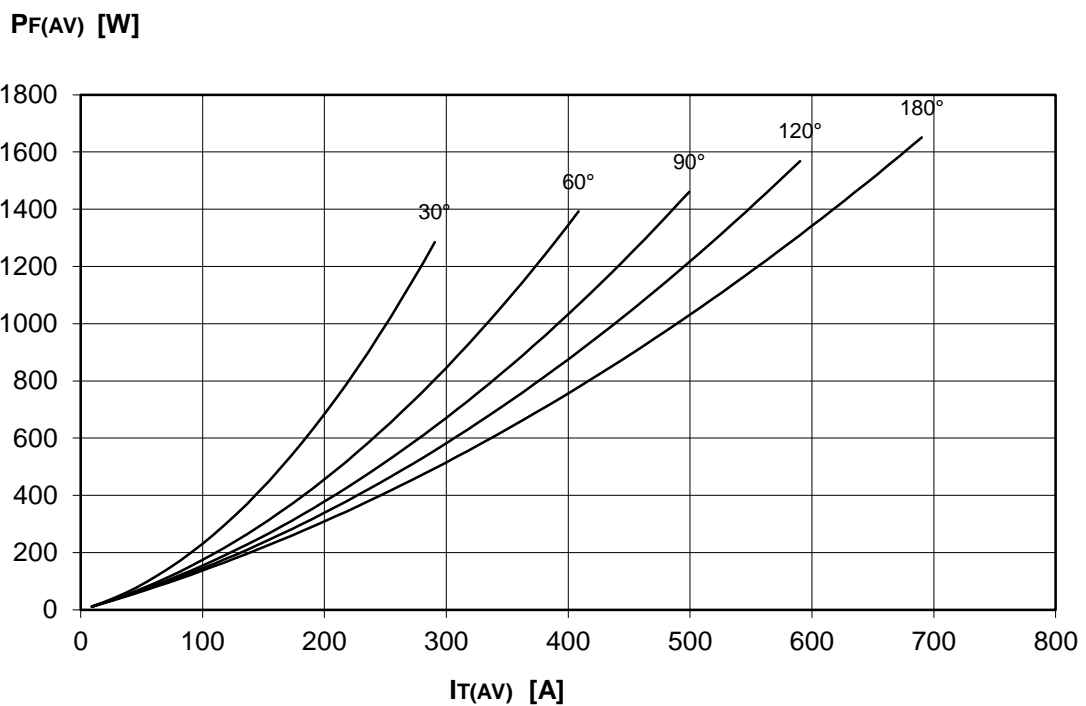
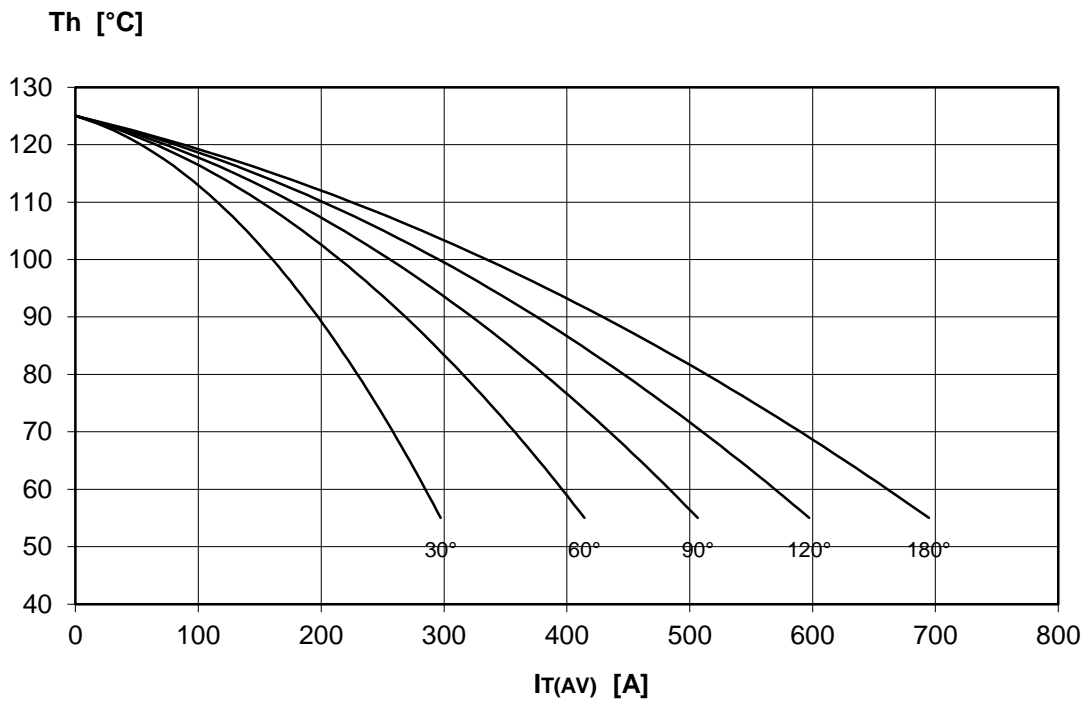
**DISSIPATION CHARACTERISTICS**

SQUARE WAVE

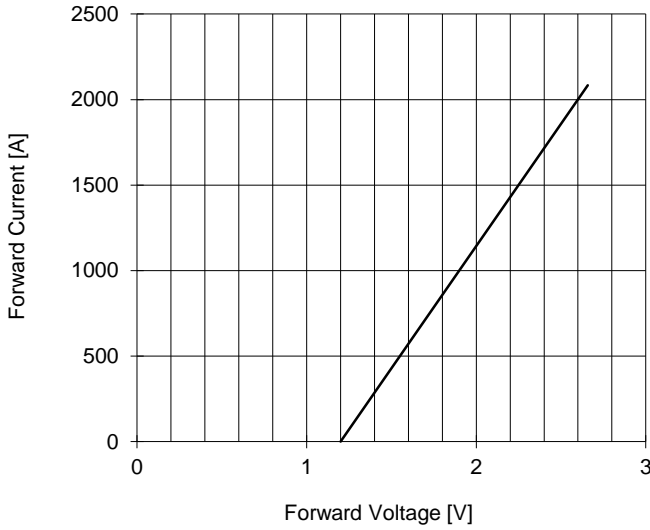


**DISSIPATION CHARACTERISTICS**

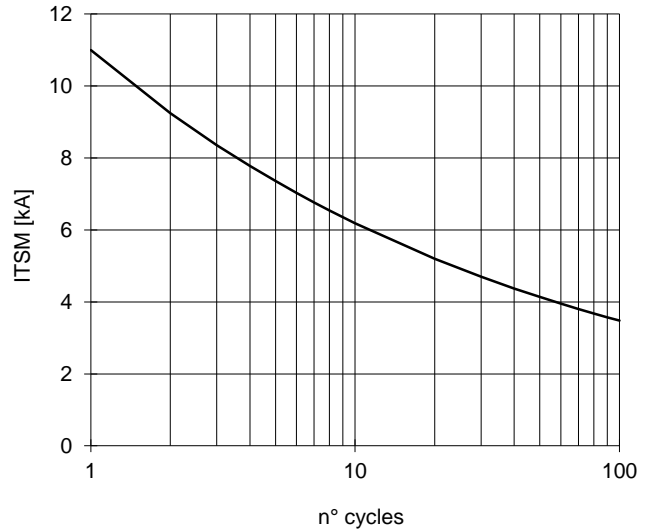
SINE WAVE



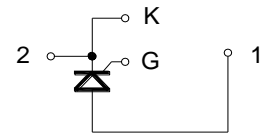
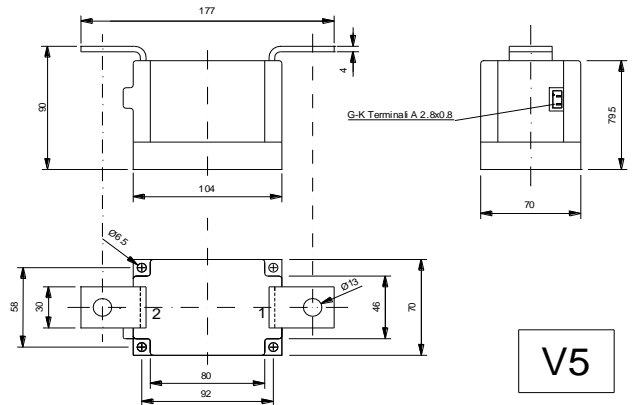
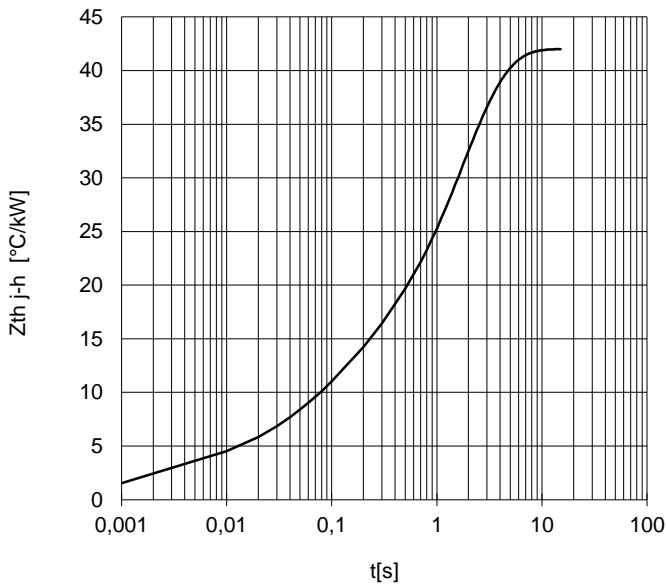
**FORWARD CHARACTERISTIC**  
T<sub>j</sub> = 125 °C



**SURGE CHARACTERISTIC**  
T<sub>j</sub> = 125 °C



**TRANSIENT THERMAL IMPEDANCE**  
DOUBLE SIDE COOLED



All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 μm. In the interest of product improvement POSEICO SpA reserves the right to change any data given in this data sheet at any time without previous notice. If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.

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