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PHASE CONTROL THYRISTOR

AT880LT

Repetitive voltage up to **5200 V**
Mean forward current **2234 A**
Surge current **48 kA**

FINAL SPECIFICATION
Nov. 20 - Issue: 0

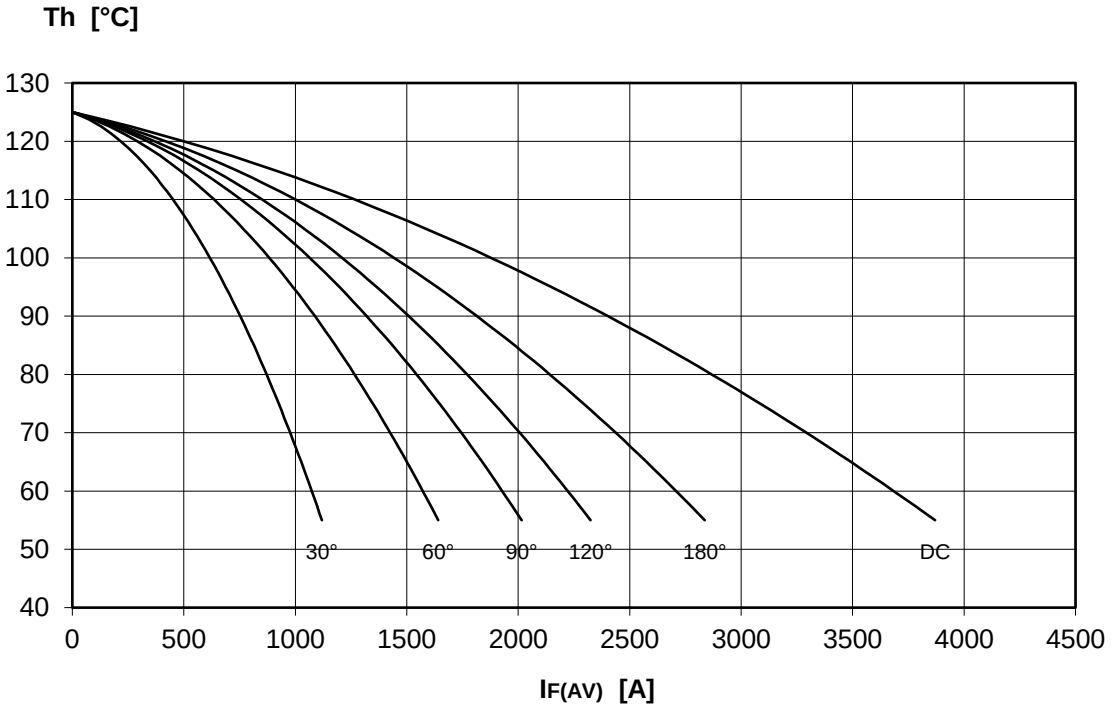
Symbol	Characteristic	Conditions	Tj [°C]	Value	Unit
BLOCKING					
V_{RRM}	Repetitive peak reverse voltage		125	5200	V
V_{RSM}	Non-repetitive peak reverse voltage		125	5300	V
V_{DRM}	Repetitive peak off-state voltage		125	5200	V
I_{RRM}	Repetitive peak reverse current	V=VRRM	125	200	mA
I_{DRM}	Repetitive peak off-state current	V=VDRM	125	200	mA
CONDUCTING					
$I_{T(AV)}$	Mean forward current	180° sin ,50 Hz, Th=55°C, double side cooled		2774	A
$I_{T(AV)}$	Mean forward current	180° sin ,50 Hz, Tc=85°C, double side cooled		2234	A
I_{TSM}	Surge forward current	Sine wave, 10 ms	125	48	kA
I^2t	I^2t	without reverse voltage		11520 x 10^3	A^2s
V_T	On-state voltage	On-state current = 3000 A	125	2.00	V
$V_{T(TO)}$	Threshold voltage		125	1.10	V
r_T	On-state slope resistance		125	0.300	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current, min.	From 67% VDRM up to 2ITAV; IG=2A	125	800	A/µs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 67% of VDRM	125	1000	V/µs
t_d	Gate controlled delay time, typical	VD=40%VDRM IT=2000A; gate pulse 2A , tgp=.50 µs	25	4	µs
t_q	Circuit commutated turn-off time, typical	dv/dt = 50 V/µs linear up to 67% VDRM		800	µs
Q_{rr}	Reverse recovery charge	di/dt = 10 A/µs, I= 2000 A	125		µC
I_{rr}	Peak reverse recovery current	VR= 100 V			A
I_H	Holding current, typical	VD=12V, gate open circuit	25	300	mA
I_L	Latching current, typical	VD=12V, tp=30µs	25	1500	mA
GATE					
V_{GT}	Gate trigger voltage	VD=12V	25	3.50	V
I_{GT}	Gate trigger current	VD=12V	25	400	mA
V_{GD}	Non-trigger gate voltage, min.	VD=VDRM	125	0.35	V
V_{FGM}	Peak gate voltage (forward)			30	V
I_{FGM}	Peak gate current			10	A
V_{RGM}	Peak gate voltage (reverse)			10	V
P_{GM}	Peak gate power dissipation	Pulse width 100 µs		150	W
P_G	Average gate power dissipation			2	W
MOUNTING					
$R_{th(j-h)}$	Thermal impedance, DC	Junction to heatsink, double side cooled		8.0	°C/kW
$R_{th(c-h)}$	Thermal impedance	Case to heatsink, double side cooled		1.5	°C/kW
T_j	Operating junction temperature			-30 / 125	°C
F	Mounting force			60.0 / 80.0	kN
	Mass			1900	g

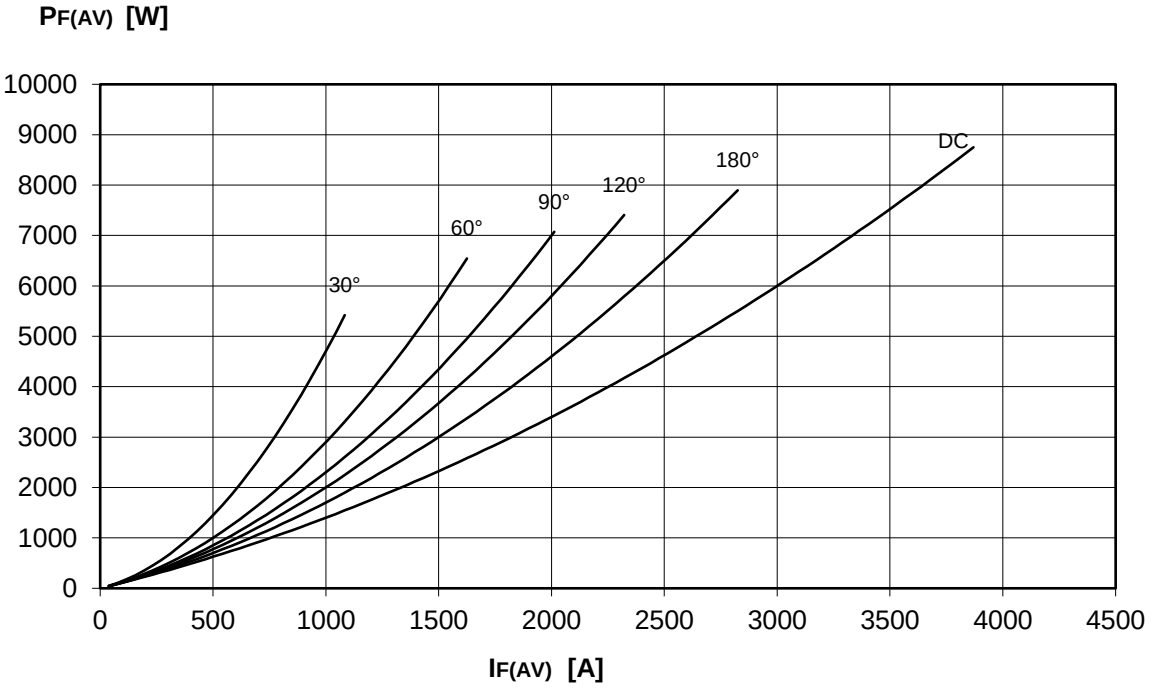
ORDERING INFORMATION : AT880LT S 52

standard specification — VRRM/100

DISSIPATION CHARACTERISTICS

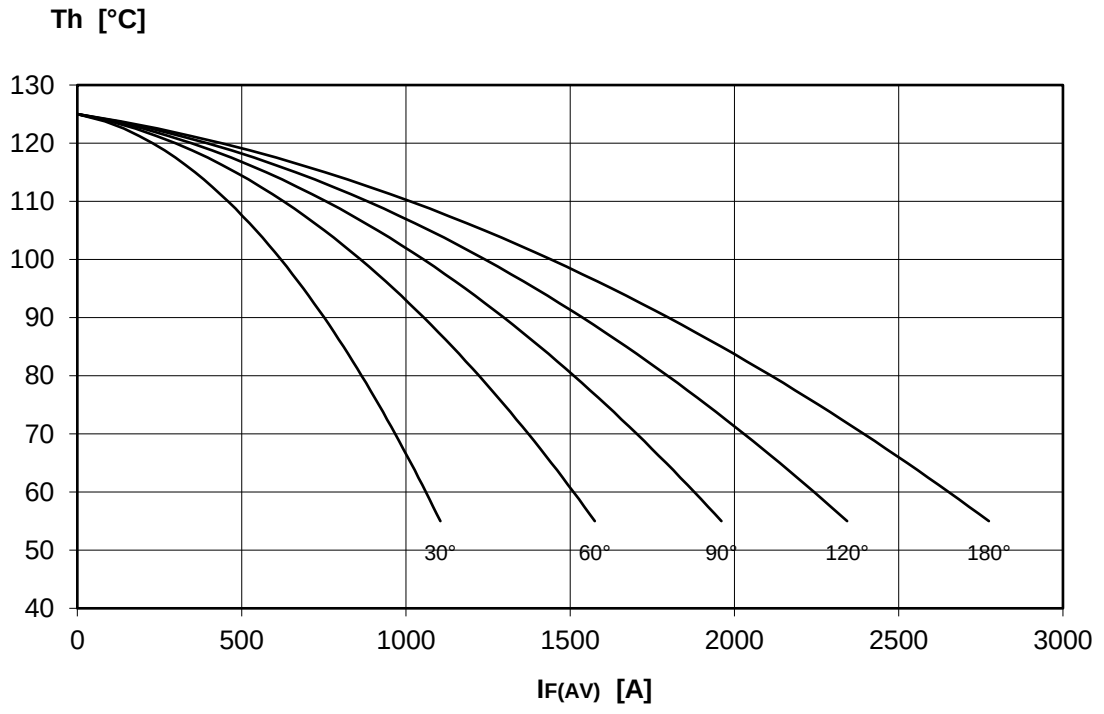
SQUARE WAVE

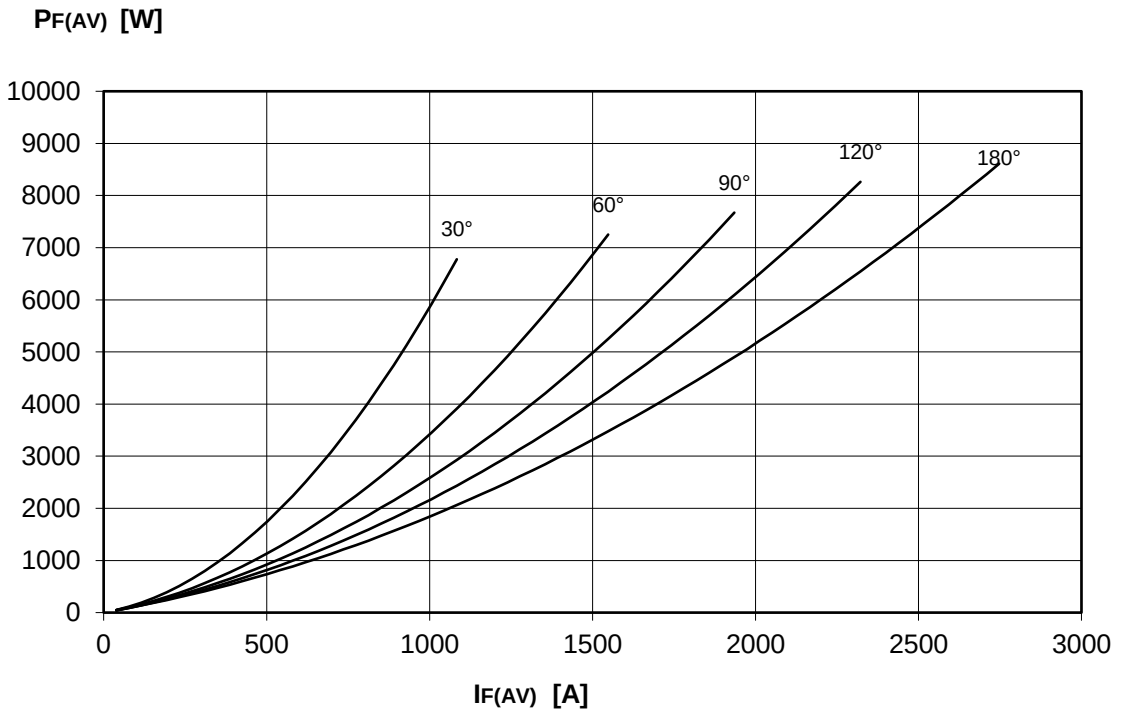




DISSIPATION CHARACTERISTICS

SINE WAVE



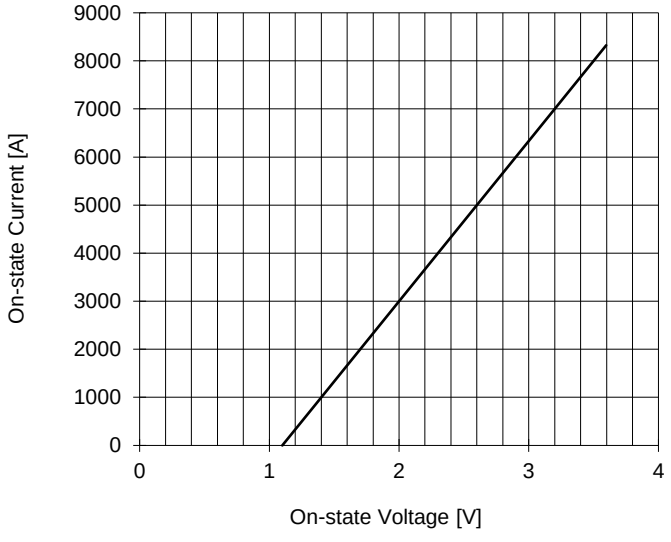


AT880LT PHASE CONTROL THYRISTOR

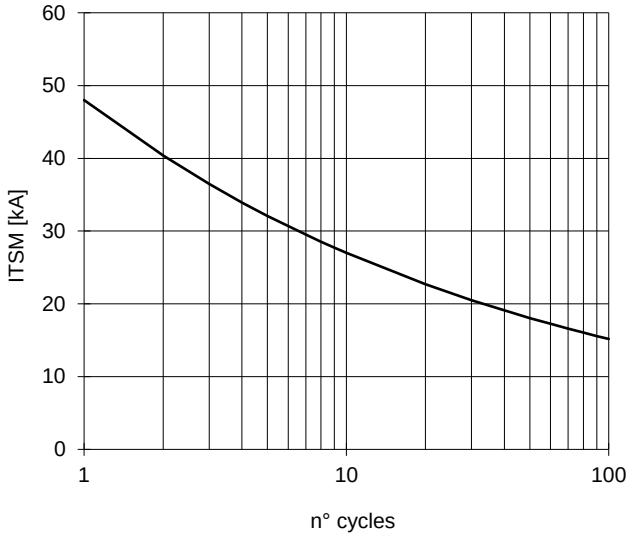
POSEICO POWER ELECTRONICS

FINAL SPECIFICATION Nov. 20 - Issue: 0

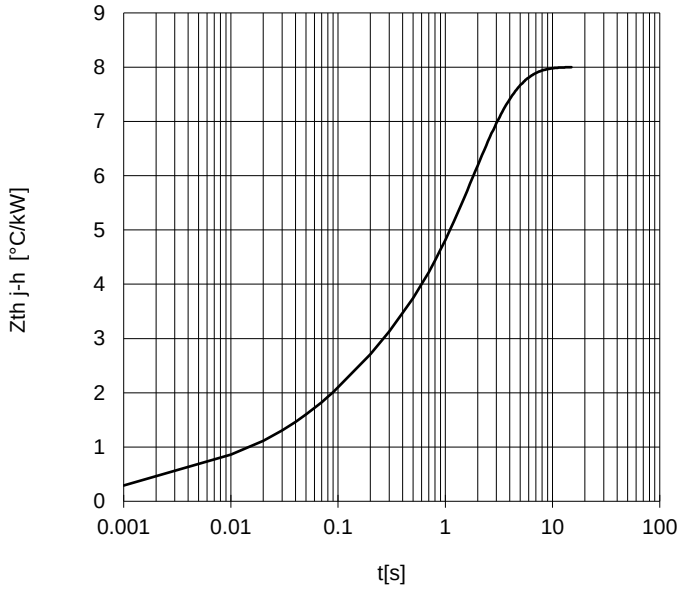
ON-STATE CHARACTERISTIC
Tj = 125 °C

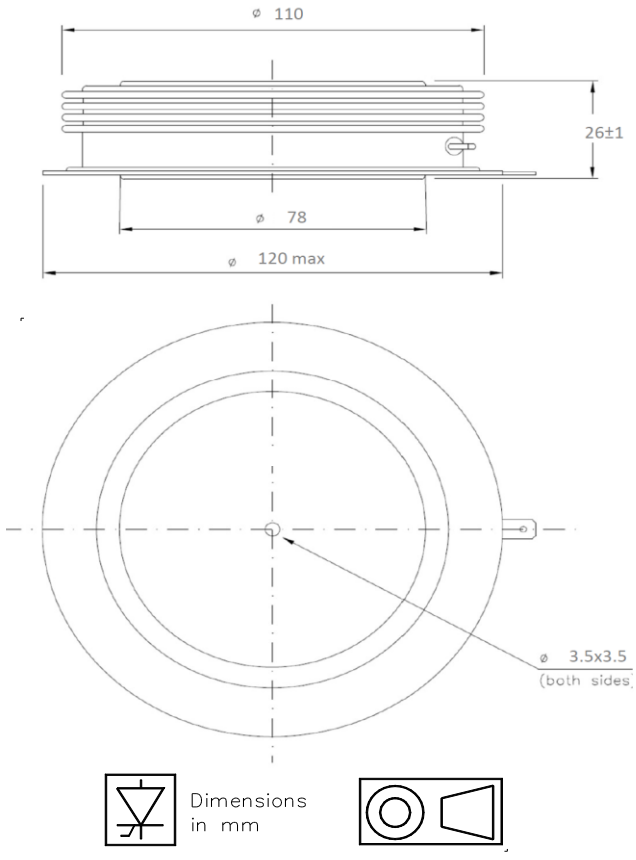


SURGE CHARACTERISTIC
Tj = 125 °C



TRANSIENT THERMAL IMPEDANCE
DOUBLE SIDE COOLED





All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 µm.
In the interest of product improvement POSEICO SpA reserves the right to change any data given in this data sheet at any time without previous notice.
If not stated otherwise the maximum value of ratings (simbols over shaded background) and characteristics is reported.

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