

## PHASE CONTROL THYRISTOR

# AT850LT

Repetitive voltage up to	<b>2800 V</b>
Mean forward current	<b>3131 A</b>
Surge current	<b>62 kA</b>

### TARGET SPECIFICATION

Dec. 19 - Issue: 0

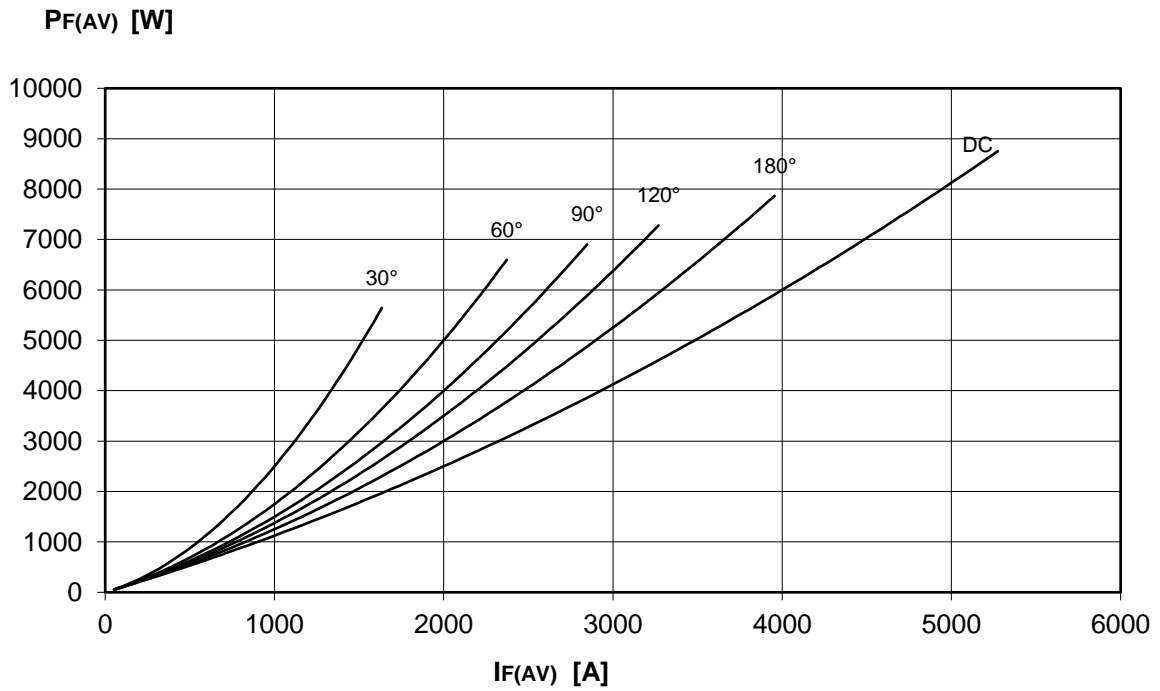
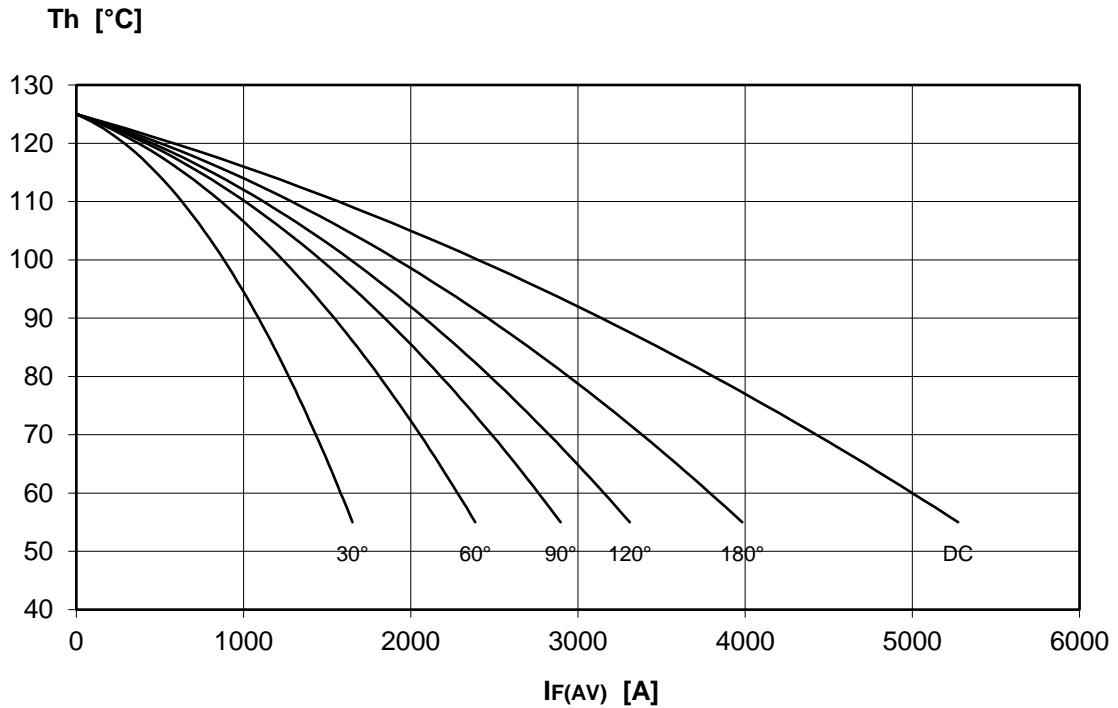
Symbol	Characteristic	Conditions	T <sub>j</sub> [°C]	Value	Unit
<b>BLOCKING</b>					
V <sub>RRM</sub>	Repetitive peak reverse voltage		125	2800	V
V <sub>RSM</sub>	Non-repetitive peak reverse voltage		125	2900	V
V <sub>DRM</sub>	Repetitive peak off-state voltage		125	2800	V
I <sub>RRM</sub>	Repetitive peak reverse current	V=VRRM	125	200	mA
I <sub>DRM</sub>	Repetitive peak off-state current	V=VDRM	125	200	mA
<b>CONDUCTING</b>					
I <sub>T(AV)</sub>	Mean forward current	180° sin ,50 Hz, Th=55°C, double side cooled		3946	A
I <sub>T(AV)</sub>	Mean forward current	180° sin ,50 Hz, Tc=85°C, double side cooled		3131	A
I <sub>TSM</sub>	Surge forward current	Sine wave, 10 ms	125	62	kA
I <sup>2</sup> t	I <sup>2</sup> t	without reverse voltage		19220 x 10 <sup>3</sup>	A <sup>2</sup> s
V <sub>T</sub>	On-state voltage	On-state current = 3000 A	125	1.20	V
V <sub>T(TO)</sub>	Threshold voltage		125	1.00	V
r <sub>T</sub>	On-state slope resistance		125	0.125	mohm
<b>SWITCHING</b>					
di/dt	Critical rate of rise of on-state current, min.	From 67% VDRM up to 2ITAV; IG=2A	125	630	A/μs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 67% of VDRM	125	1000	V/μs
t <sub>d</sub>	Gate controlled delay time, typical	VD=40%VDRM IT=2000A; gate pulse 2A , tgp=.50 μs	25	4	μs
t <sub>q</sub>	Circuit commutated turn-off time, typical	dv/dt = 50 V/μs linear up to 67% VDRM		400	μs
Q <sub>rr</sub>	Reverse recovery charge	di/dt = 10 A/μs, I = 2000 A	125		μC
I <sub>rr</sub>	Peak reverse recovery current	VR= 100 V			A
I <sub>H</sub>	Holding current, typical	VD=12V, gate open circuit	25	300	mA
I <sub>L</sub>	Latching current, typical	VD=12V, tp=30μs	25	1500	mA
<b>GATE</b>					
V <sub>GT</sub>	Gate trigger voltage	VD=12V	25	3.50	V
I <sub>GT</sub>	Gate trigger current	VD=12V	25	400	mA
V <sub>GD</sub>	Non-trigger gate voltage, min.	VD=VDRM	125	0.35	V
V <sub>FGM</sub>	Peak gate voltage (forward)			30	V
I <sub>FGM</sub>	Peak gate current			10	A
V <sub>RGM</sub>	Peak gate voltage (reverse)			10	V
P <sub>GM</sub>	Peak gate power dissipation	Pulse width 100 μs		150	W
P <sub>G</sub>	Average gate power dissipation			2	W
<b>MOUNTING</b>					
R <sub>th(j-h)</sub>	Thermal impedance, DC	Junction to heatsink, double side cooled		8.0	°C/kW
R <sub>th(c-h)</sub>	Thermal impedance	Case to heatsink, double side cooled		1.5	°C/kW
T <sub>j</sub>	Operating junction temperature			-30 / 125	°C
F	Mounting force			60.0 / 80.0	kN
	Mass			1900	g

ORDERING INFORMATION : AT850LT S 28

standard specification   VRRM/100

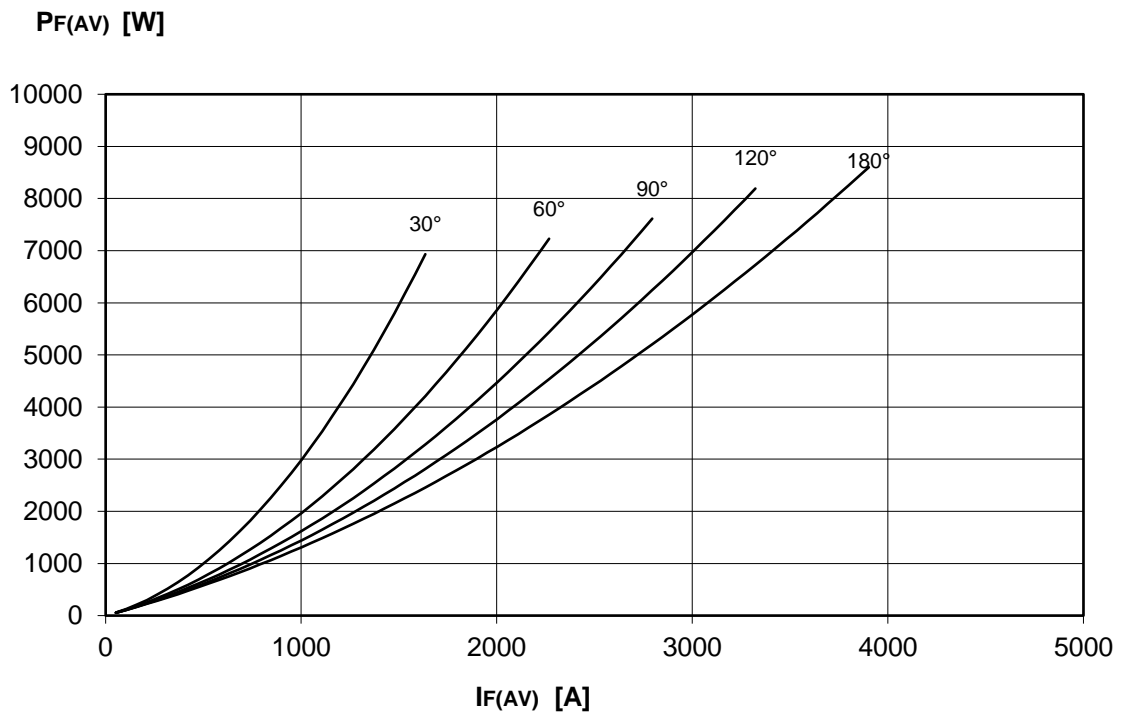
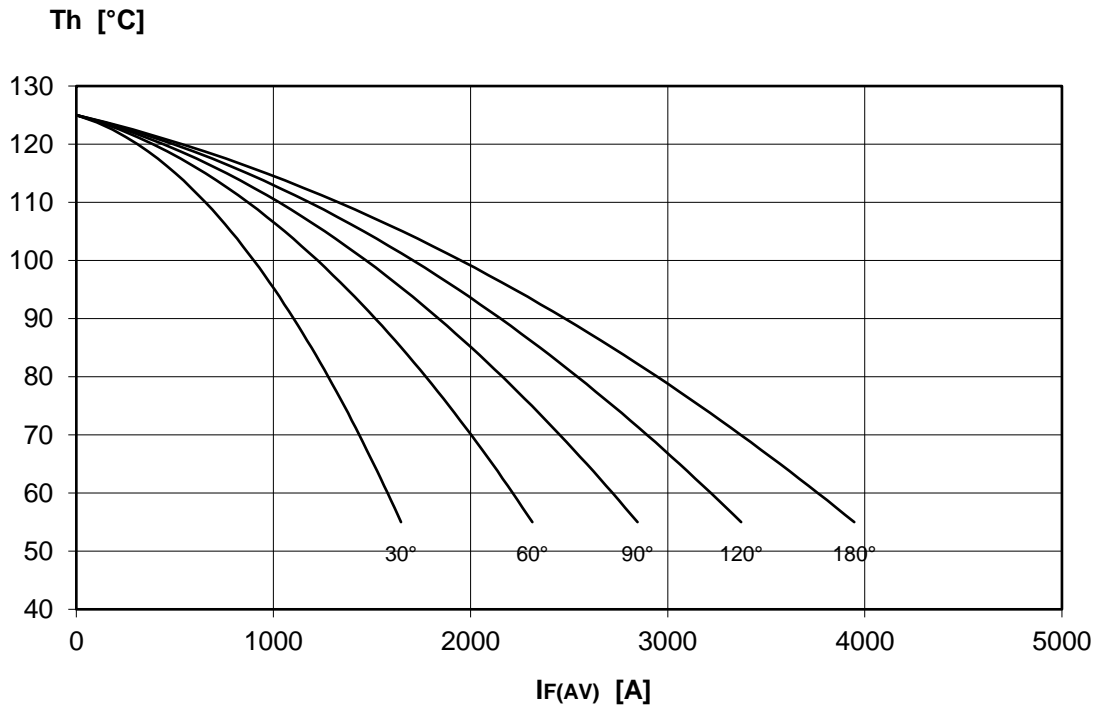
DISSIPATION CHARACTERISTICS

SQUARE WAVE



DISSIPATION CHARACTERISTICS

SINE WAVE

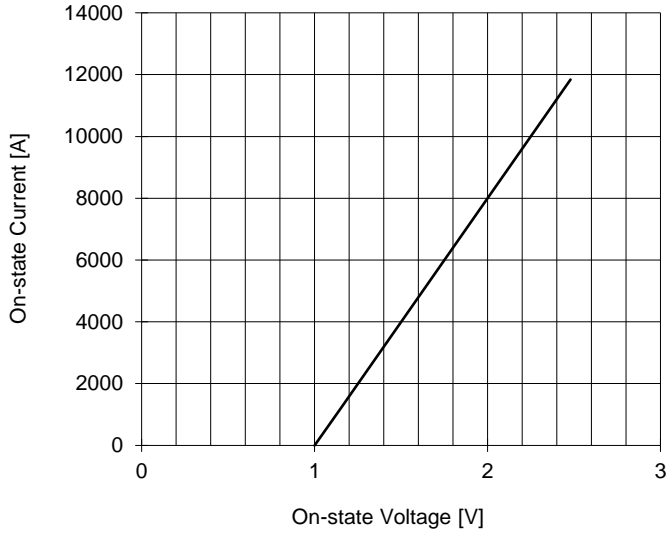


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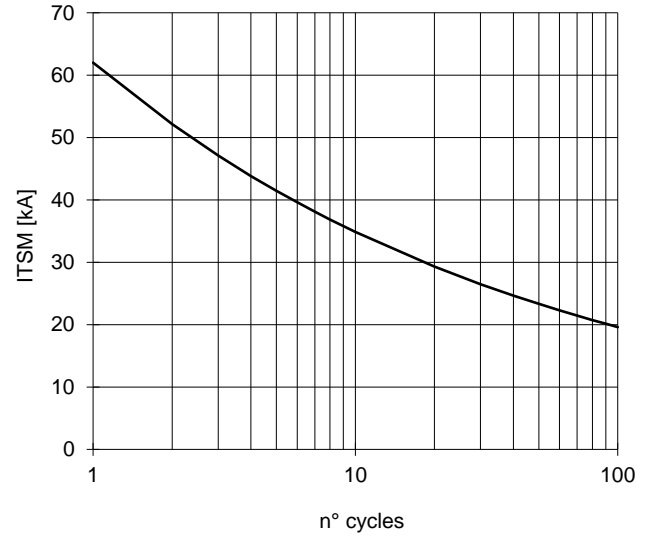


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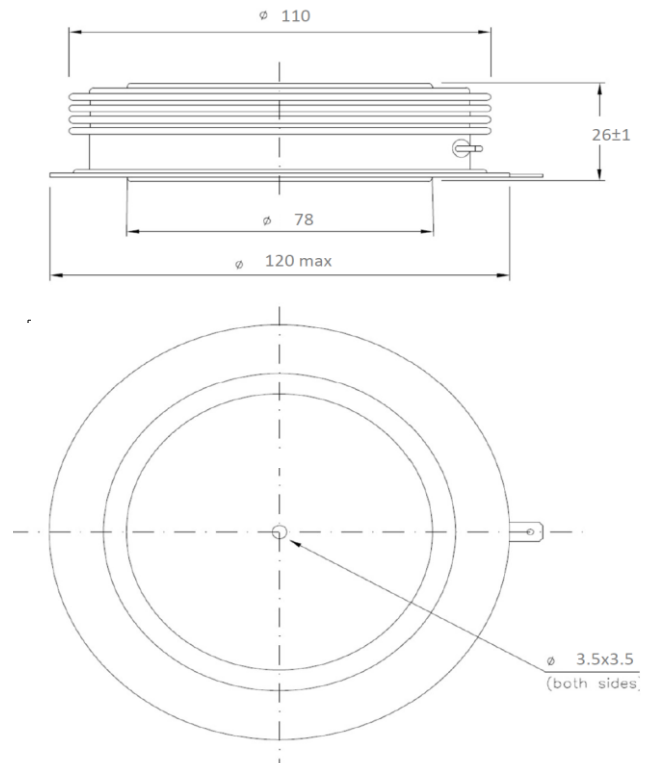
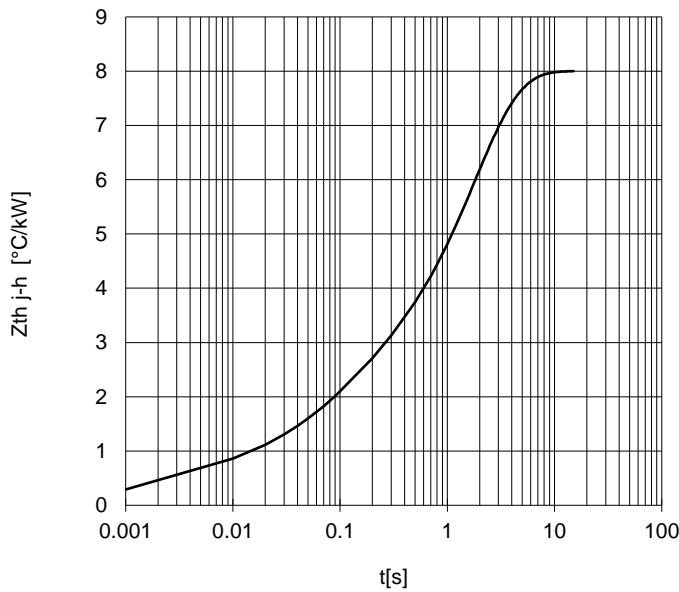
ON-STATE CHARACTERISTIC  
T<sub>j</sub> = 125 °C



SURGE CHARACTERISTIC  
T<sub>j</sub> = 125 °C



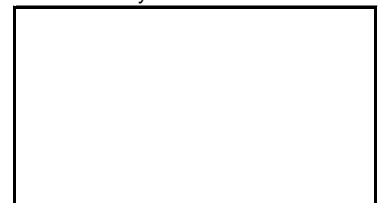
TRANSIENT THERMAL IMPEDANCE  
DOUBLE SIDE COOLED



Dimensions  
in mm



Distributed by



All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 μm. In the interest of product improvement POSEICO SpA reserves the right to change any data given in this data sheet at any time without previous notice. If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.