POSEICO
POWER ELECTRONICS

PHASE CONTROL THYRISTOR
AT607

Repetitive Voltage	**200-800**	**V**
Mean Forward Current	**2585**	**A**
Surge Current	**36**	**kA**
Treeshold Voltage	**0.8**	**V**
On-State Resistance	**0.12**	**mΩ**

Ordering Information	VDRM/VRRM [V]
AT607 S2	200
AT607 S4	400
AT607 S6	600
AT607 S8	800

S= standard specification
P= for parallel application

FINAL SPECIFICATION

June 25 - Issue: 10

Symbol	Characteristic	Conditions	Tj [°C]	Value	Unit
BLOCKING					
V_{RRM}	Repetitive peak reverse voltage		140	200-800	V
V_{RSM}	Non-repetitive peak reverse voltage		140	300-900	V
V_{DRM}	Repetitive peak off-state voltage		140	200-800	V
I_{RRM}	Repetitive peak reverse current	V=VRRM	140	100	mA
I_{DRM}	Repetitive peak off-state current	V=VDRM	140	100	mA
CONDUCTING					
$I_{T(AV)}$	Mean forward current	180° sin, 50 Hz, Th=55°C, double side cooled		2585	A
$I_{T(AV)}$	Mean forward current	180° sin, 50 Hz, Tc=85°C, double side cooled		2419	A
I_{TSM}	Surge forward current	Sine wave, 10 ms	140	36	kA
I^2t	I^2t	without reverse voltage		6480 x 10^3	A^2s
V_T	On-state voltage	On-state current = 6000 A	25	1.55	V
$V_{T(TO)}$	Threshold voltage		140	0.80	V
r_T	On-state slope resistance		140	0.120	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current, min.	From 75% VDRM up to 2200 A; gate 10V, 5Ω	140	200	A/µs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of VDRM	140	500	V/µs
t_d	Gate controlled delay time, typical	VD=100V; gate source 25V, 10Ω , tr=.5 µs	25	3.0	µs
t_q	Circuit commutated turn-off time, typical	dv/dt = 20 V/µs linear up to 75% VDRM		250	µs
Q_{rr}	Reverse recovery charge	di/dt = -20 A/µs, I= 1430 A	140		µC
I_{rr}	Peak reverse recovery current	VR= 50 V			A
I_H	Holding current, typical	VD=5V, gate open circuit	25	300	mA
I_L	Latching current, typical	VD=5V, tp=30µs	25	700	mA
GATE					
V_{GT}	Gate trigger voltage	VD=5V	25	3.50	V
I_{GT}	Gate trigger current	VD=5V	25	300	mA
V_{GD}	Non-trigger gate voltage, min.	VD=VDRM	140	0.25	V
V_{FGM}	Peak gate voltage (forward)			30	V
I_{FGM}	Peak gate current			10	A
V_{RGM}	Peak gate voltage (reverse)			5	V
P_{GM}	Peak gate power dissipation	Pulse width 100 µs		150	W
P_G	Average gate power dissipation			2	W
MOUNTING					
$R_{th(j-h)}$	Thermal impedance, DC	Junction to heatsink, double side cooled		21.0	°C/kW
$R_{th(c-h)}$	Thermal impedance	Case to heatsink, double side cooled		6.0	°C/kW
T_j	Operating junction temperature			-30 / 140	°C
F	Mounting force			22 / 26	kN
	Mass			520	g

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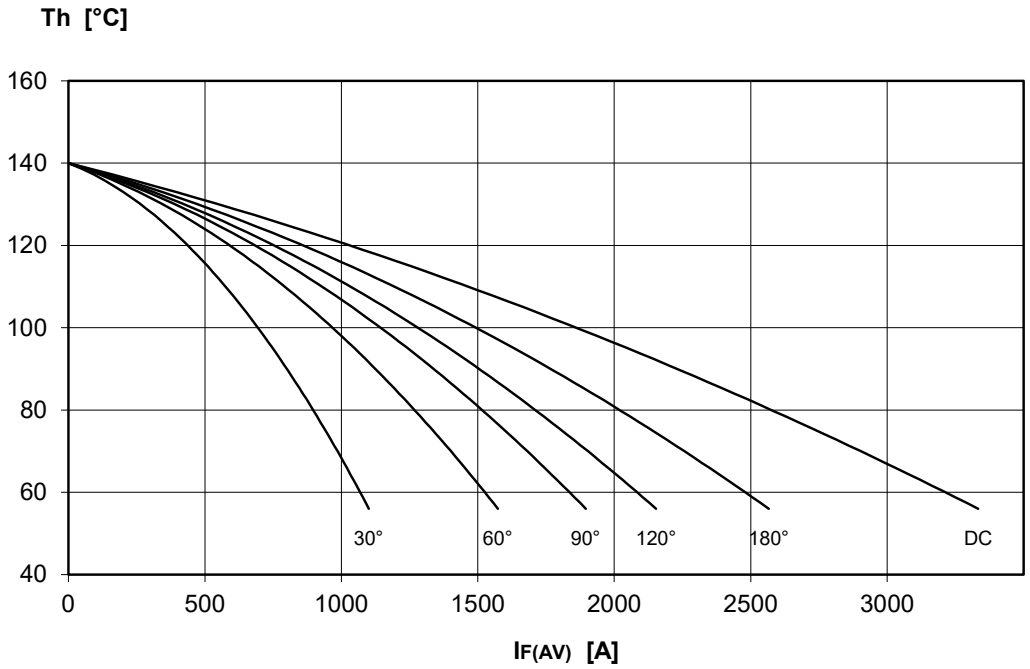
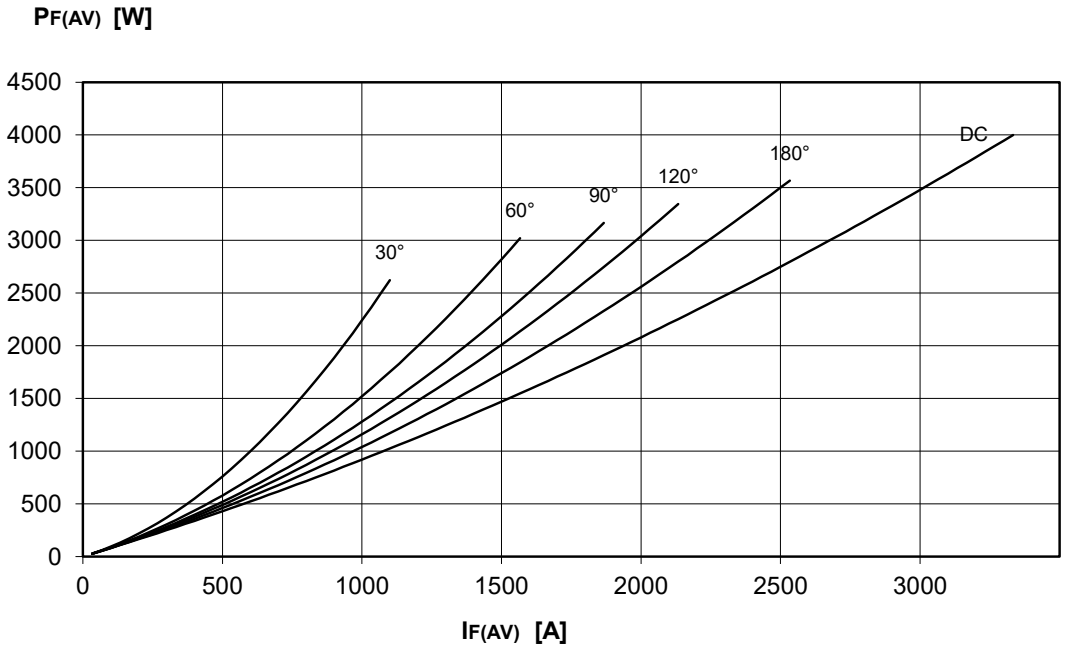
DISSIPATION CHARACTERISTICS

SQUARE WAVE





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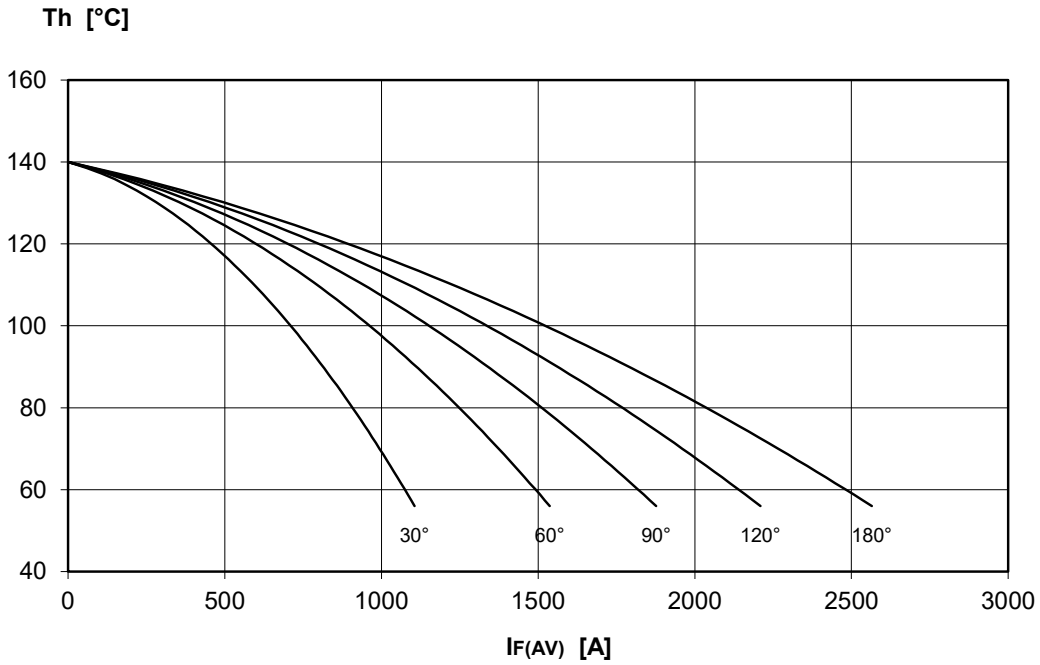
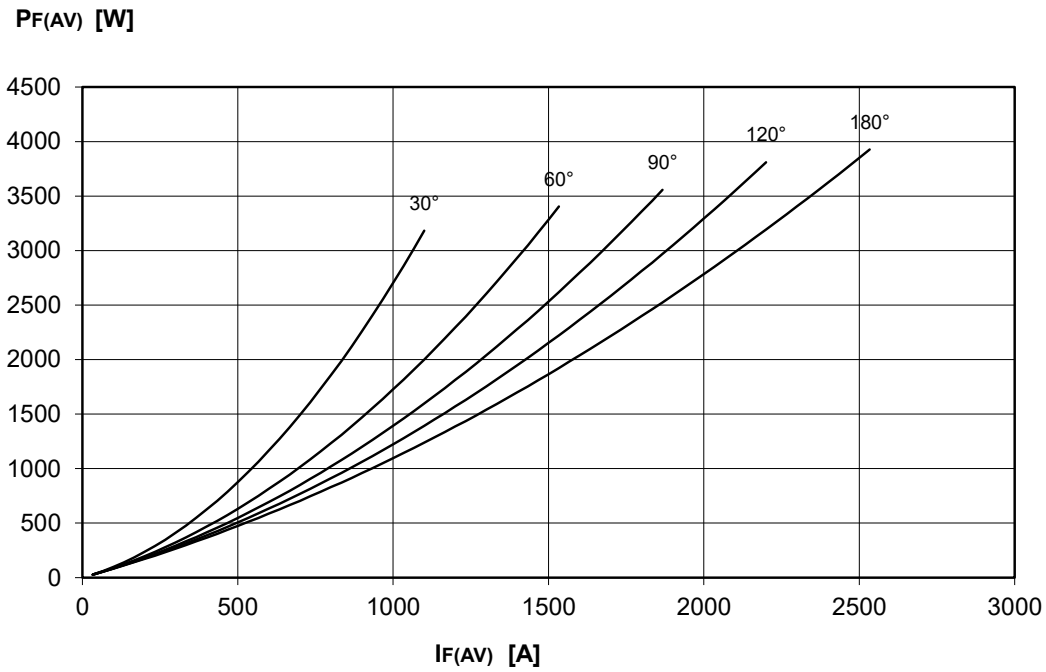
DISSIPATION CHARACTERISTICS

SINE WAVE





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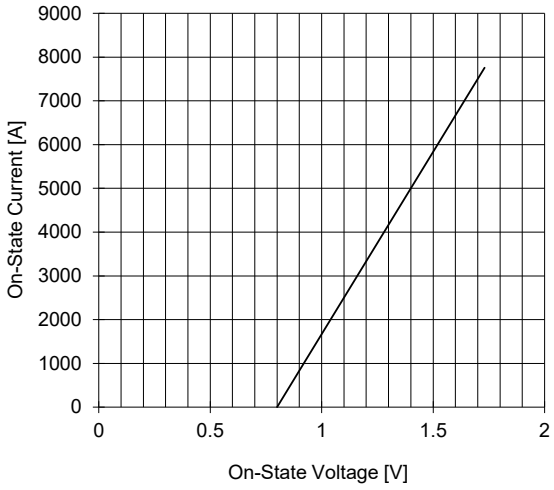
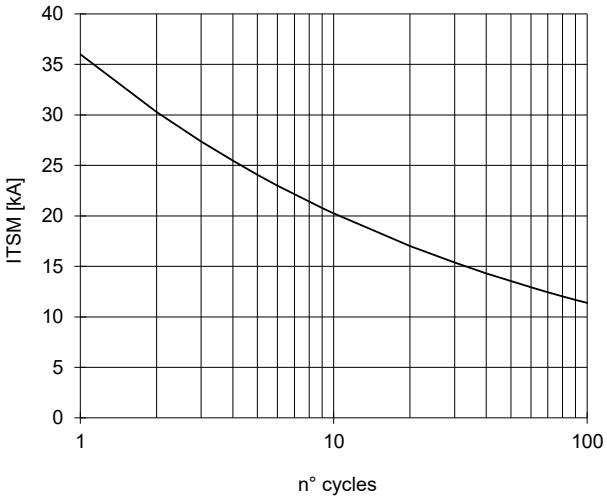
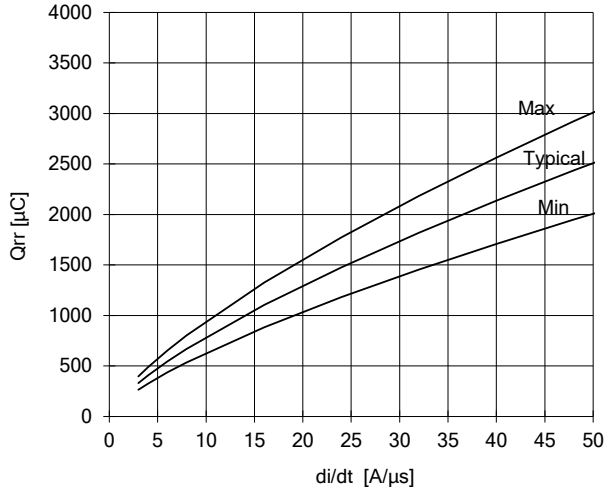
ON-STATE CHARACTERISTIC
Tj = 140 °C



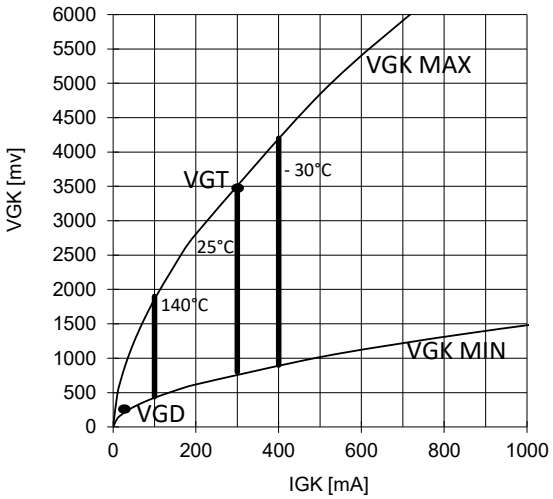
SURGE CHARACTERISTIC
Tj = 140 °C



REVERSE RECOVERY CHARGE
@ TJ=140 °C; IT = 1000 A



GATE TRIGGER CHARACTERISTICS



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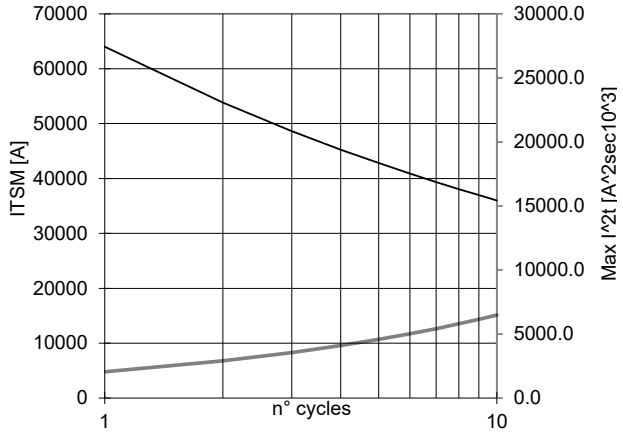
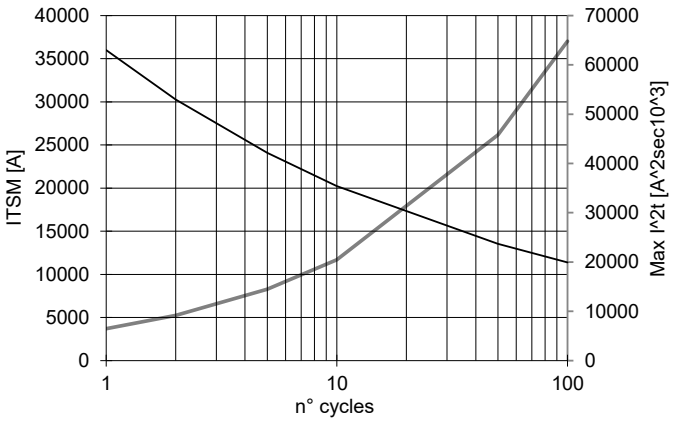
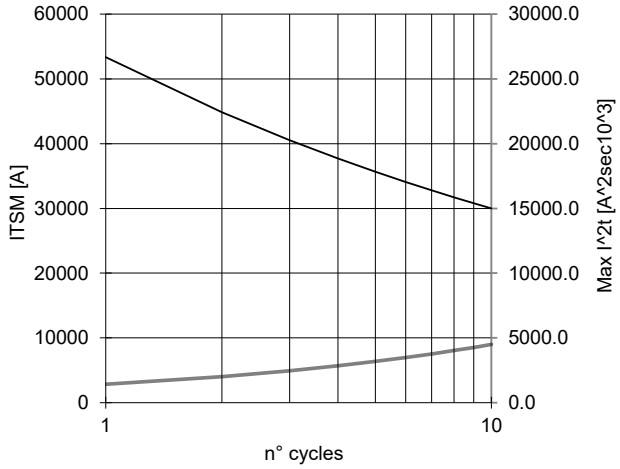
ITSM - I^2t CHARACTERISTIC
@ 1 - 10 ms; VR=0



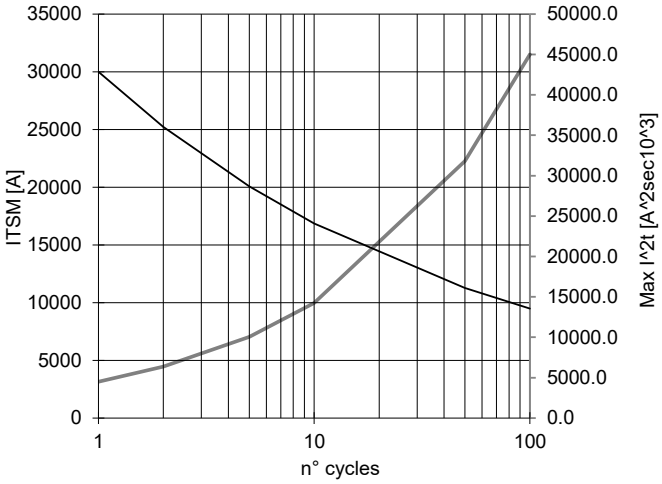
ITSM - I^2T VS NUMBER OF 10 MS PULSE
VR=0



ITSM - I^2t CHARACTERISTIC
@ 1 - 10 ms; VR=60%VRRM



ITSM - I^2T VS NUMBER OF 10 MS PULSE
VR=60%VRRM



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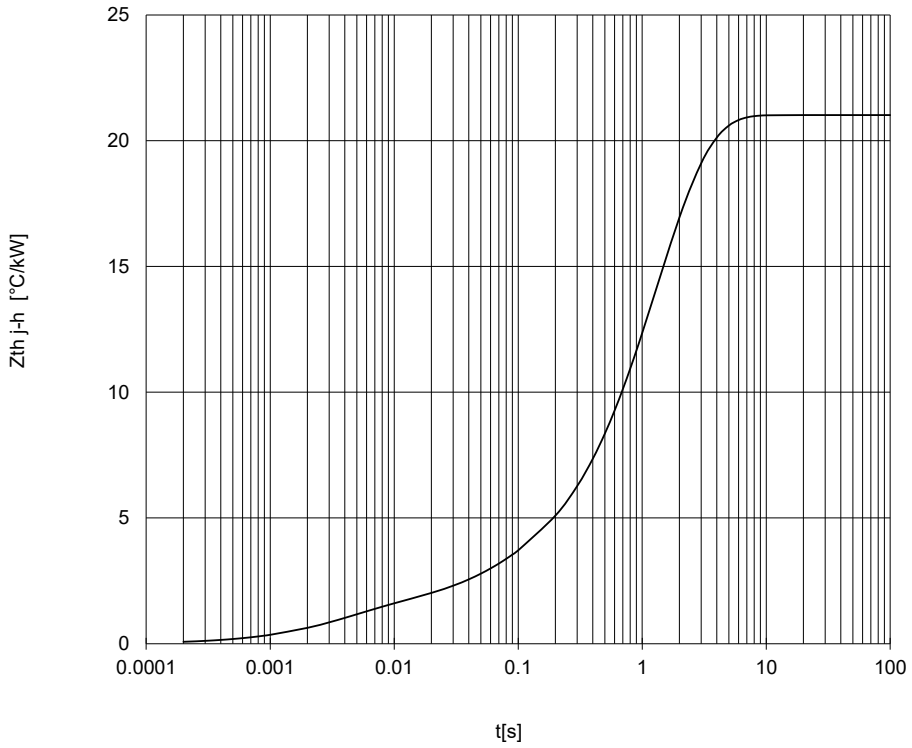
TRANSIENT THERMAL IMPEDANCE Zth j-h
DOUBLE SIDE COOLED



$$Z_{th\ j-h}(t) = \sum_{i=1}^{n} A_i * \left(1 - e^{-\frac{t}{\tau_i}}\right)$$

0	1	2	3	4
A_i [°C/kW]	18.50	1.12	0.90	0.50
τ_i [s]	1.3200	0.0510	0.0032	0.0059

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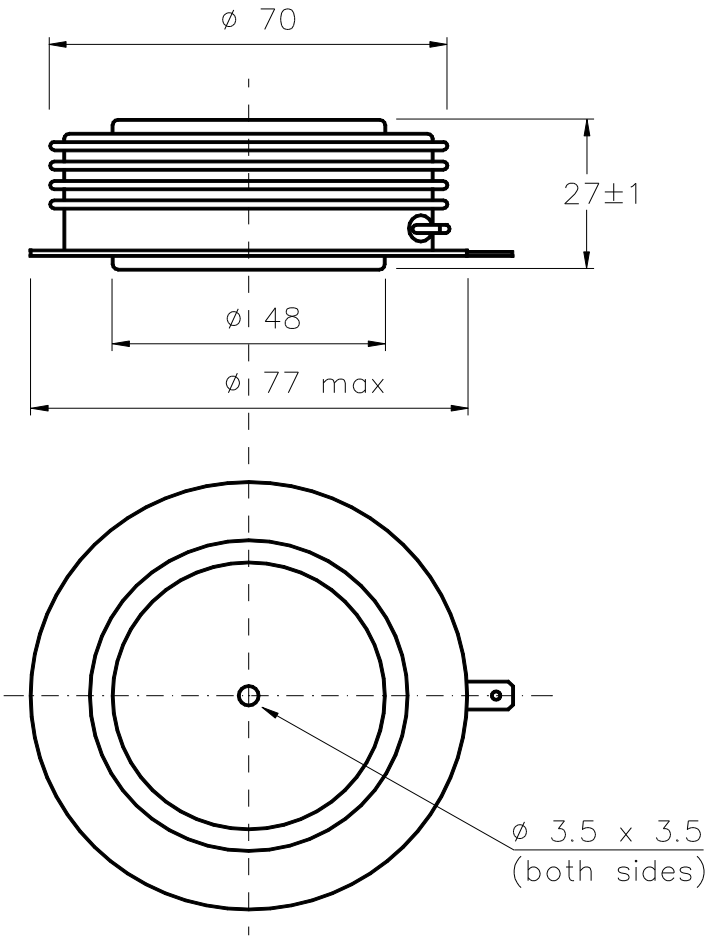

Cathode terminal type DIN 46244 - A 4.8 - 0.8

Gate terminal type AMP 60598 - 1

DISCLAIMER: All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 µm. The tolerance of the drawing is ± 1 mm

In the interest of product improvement POSEICO SpA reserves the right to change any data given in this data sheet at any time without previous notice.

If not stated otherwise the maximum value of ratings (simbols over shaded background) and characteristics is reported.

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