POSEICO SPA
Via Pillea 42-44, 16153 Genova - ITALY
Tel. + 39 010 8599400 - Fax + 39 010 8682006
Sales Office:
Tel. + 39 010 8599400 - Fax + 39 010 8681180

FAST SWITCHING THYRISTOR

ATF587

Repetitive voltage up to	**1200 V**
Mean on-state current	**350 A**
Surge current	**4,5 kA**
Turn-off time	**25 µs**

FINAL SPECIFICATION

gen 18 - ISSUE : 5

Symbol	Characteristic	Conditions	Tj [°C]	Value	Unit
BLOCKING					
V_{RRM}	Repetitive peak reverse voltage		125	1200	V
V_{RSM}	Non-repetitive peak reverse voltage		125	1300	V
V_{DRM}	Repetitive peak off-state voltage		125	1200	V
I_{RRM}	Repetitive peak reverse current	V=VRRM	125	40	mA
I_{DRM}	Repetitive peak off-state current	V=VDRM	125	40	mA
CONDUCTING					
$I_{T(AV)}$	Mean on-state current	180° sin, 50 Hz, Th=55°C, double side cooled		350	A
$I_{T(AV)}$	Mean on-state current	180° sin, 500 Hz, Th=55°C, double side cooled		315	A
I_{TSM}	Surge on-state current, non repetitive	sine wave, 10 ms	125	4,5	kA
I^2t	I^2t	without reverse voltage		101 x1E3	A^2s
V_T	On-state voltage	On-state current = 800 A	25	2,15	V
$V_{T(TO)}$	Threshold voltage		125	1,38	V
r_T	On-state slope resistance		125	0,830	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current, min	From 75% VDRM up to 900 A, gate 20V 10 ohm	125	200	A/µs
dv/dt	Critical rate of rise of off-state voltage, min	Linear ramp up to 70% of VDRM	125	500	V/µs
td	Gate controlled delay time, typical	VD=100V, gate source 20V, 10 ohm , tr=1 µs	25	0,4	µs
tq	Circuit commutated turn-off time	di/dt = 20 A/µs, I = 250 A dV/dt = 200 V/µs , up to 75% VDRM	125	25	µs
Q_{rr}	Reverse recovery charge	di/dt = 60 A/µs, I = 1000 A	125	190	µC
I_{rr}	Peak reverse recovery current	VR = 50 V		139	A
I_H	Holding current, typical	VD=5V, gate open circuit	25	45	mA
I_L	Latching current, typical	VD=12V, tp=30µs	25	70	mA
GATE					
V_{GT}	Gate trigger voltage	VD=5V	25	3,5	V
I_{GT}	Gate trigger current	VD=5V	25	350	mA
V_{GD}	Non-trigger gate voltage, min.	VD=VDRM	125	0,25	V
V_{FGM}	Peak gate voltage (forward)		25	30	V
I_{FGM}	Peak gate current		25	10	A
V_{RGM}	Peak gate voltage (reverse)		25	5	V
P_{GM}	Peak gate power dissipation	Pulse width 100 µs	25	150	W
$P_{G(AV)}$	Average gate power dissipation		25	3	W
MOUNTING					
$R_{th(j-h)}$	Thermal impedance, DC	Junction to heatsink, double side cooled		95	°C/kW
T_j	Operating junction temperature			-30 / 125	°C
F	Mounting force			4.5 / 5.0	kN
	Mass			55	g

ORDERING INFORMATION : ATF587 S 12 L — tq code; standard specification; VDRM&VRRM/100

tq code

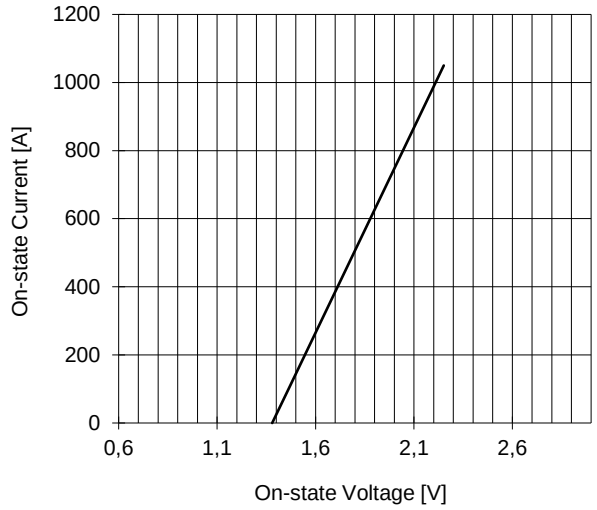
D 10 µs	C 12 µs	B 15 µs	A 20 µs	L 25 µs
M 30 µs	N 35 µs	P 40 µs	R 45 µs	S 50 µs
T 60 µs	U 70 µs	W 80 µs	X 100µs	Y 150µs

ATF587 FAST SWITCHING THYRISTOR

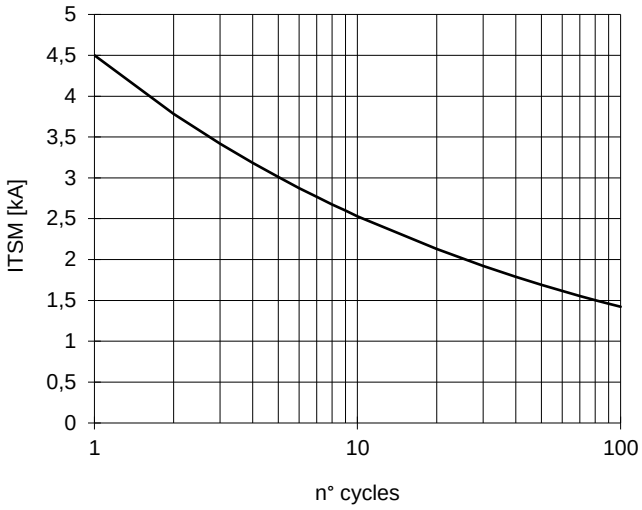
POSEICO POWER ELECTRONICS

FINAL SPECIFICATION gen 18 - ISSUE : 5

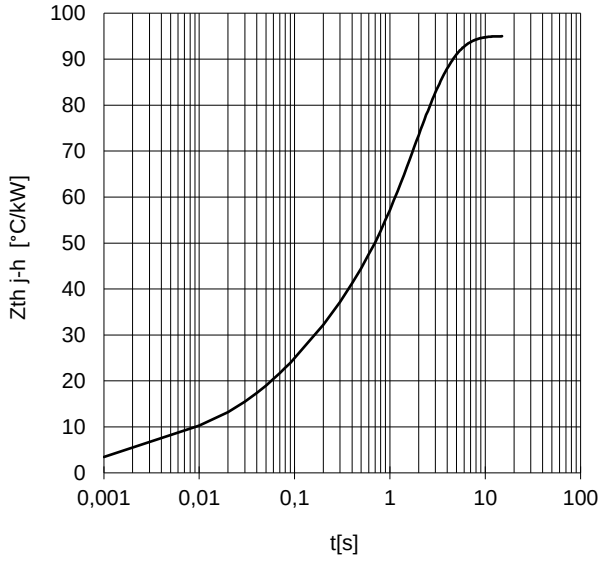
ON-STATE CHARACTERISTIC
Tj = 125 °C

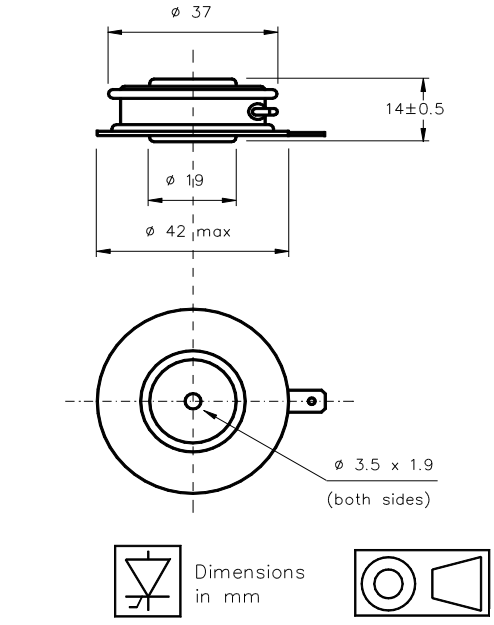


SURGE CHARACTERISTIC
Tj = 125 °C



TRANSIENT THERMAL IMPEDANCE
DOUBLE SIDE COOLED





Cathode terminal type DIN 46244 - A 4.8 - 0.8
Gate terminal type AMP 60598 - 1

All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 µm.
In the interest of product improvement POSEICO SpA reserves the right to change any data given in this data sheet at any time without previous notice.
If not stated otherwise the maximum value of ratings (simbols over shaded background) and characteristics is reported.

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