

FAST SWITCHING THYRISTOR

ATF585

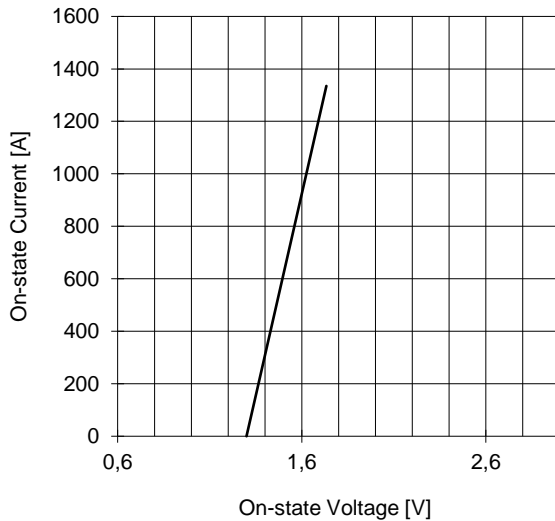
Repetitive voltage up to **800 V**
Mean on-state current **445 A**
Surge current **6 kA**
Turn-off time **15 μ s**

FINAL SPECIFICATION

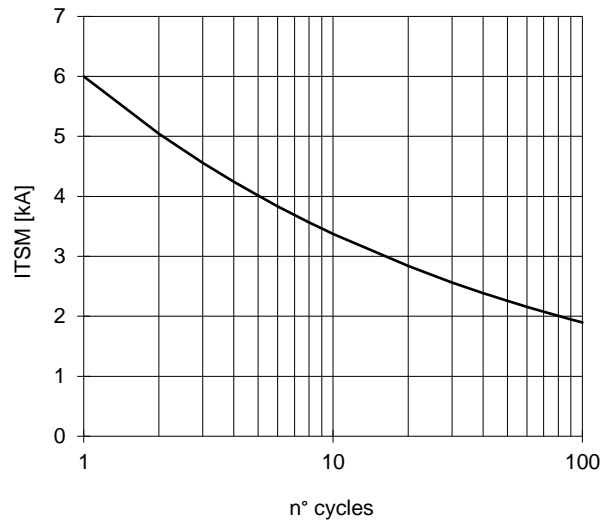
gen 18 - ISSUE : 04

Symbol	Characteristic	Conditions	T _j [°C]	Value	Unit
BLOCKING					
V _{RRM}	Repetitive peak reverse voltage		125	800	V
V _{RSM}	Non-repetitive peak reverse voltage		125	900	V
V _{DRM}	Repetitive peak off-state voltage		125	800	V
I _{RRM}	Repetitive peak reverse current	V=VRRM	125	40	mA
I _{DRM}	Repetitive peak off-state current	V=VDRM	125	40	mA
CONDUCTING					
I _{T(AV)}	Mean on-state current	180° sin, 50 Hz, Th=55°C, double side cooled		445	A
I _{T(AV)}	Mean on-state current	180° sin, 1 kHz, Th=55°C, double side cooled		400	A
I _{TSM}	Surge on-state current, non repetitive	sine wave, 10 ms	125	6	kA
I ² t	I ² t	without reverse voltage		180 x1E3	A ² s
V _T	On-state voltage	On-state current = 800 A	25	1,7	V
V _{T(TO)}	Threshold voltage		125	1,30	V
r _T	On-state slope resistance		125	0,325	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current, min	From 75% VDRM up to 1200 A, gate 20V 10 ohm	125	200	A/ μ s
dv/dt	Critical rate of rise of off-state voltage, min	Linear ramp up to 70% of VDRM	125	500	V/ μ s
t _d	Gate controlled delay time, typical	VD=100V, gate source 20V, 10 ohm , tr=1 μ s	25	0,6	μ s
t _q	Circuit commutated turn-off time	di/dt = 20 A/ μ s, I = 250 A dV/dt = 200 V/ μ s , up to 75% VDRM	125	15	μ s
Q _{rr}	Reverse recovery charge	di/dt = 60 A/ μ s, I = 1000 A	125	140	μ C
I _{rr}	Peak reverse recovery current	VR = 50 V		104	A
I _H	Holding current, typical	VD=5V, gate open circuit	25	75	mA
I _L	Latching current, typical	VD=12V, tp=30 μ s	25	150	mA
GATE					
V _{GT}	Gate trigger voltage	VD=5V	25	3,5	V
I _{GT}	Gate trigger current	VD=5V	25	350	mA
V _{GD}	Non-trigger gate voltage, min.	VD=VDRM	125	0,25	V
V _{FGM}	Peak gate voltage (forward)		25	25	V
I _{FGM}	Peak gate current		25	8	A
V _{RGM}	Peak gate voltage (reverse)		25	5	V
P _{GM}	Peak gate power dissipation	Pulse width 100 μ s	25	100	W
P _{G(AV)}	Average gate power dissipation		25	1	W
MOUNTING					
R _{th(j-h)}	Thermal impedance, DC	Junction to heatsink, double side cooled		95	°C/kW
T _j	Operating junction temperature			-30 / 125	°C
F	Mounting force			4.5 / 5.0	kN
	Mass			55	g
ORDERING INFORMATION : ATF585 S 08 B _____ tq code					
standard specification _____ VDRM&VRRM/100					
			tq code		
D 10 μ s	C 12 μ s	B 15 μ s	A 20 μ s	L 25 μ s	
M 30 μ s	N 35 μ s	P 40 μ s	R 45 μ s	S 50 μ s	
T 60 μ s	U 70 μ s	W 80 μ s	X 100 μ s	Y 150 μ s	

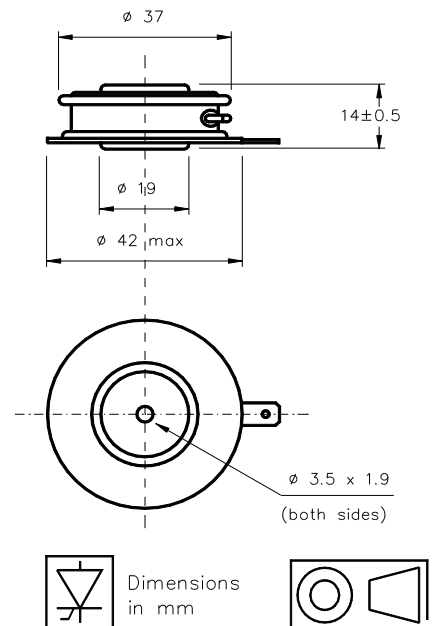
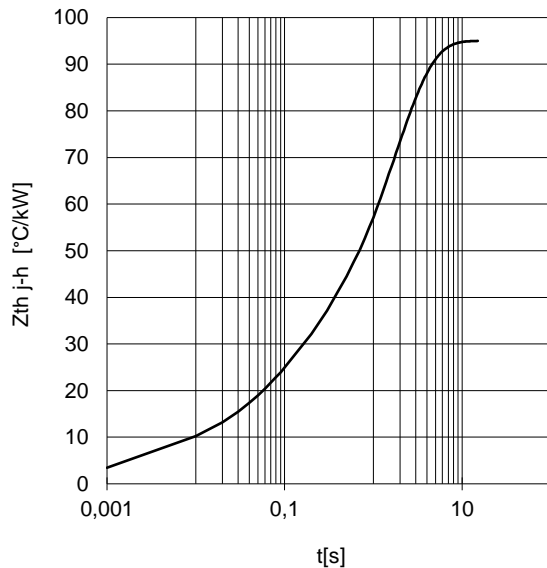
ON-STATE CHARACTERISTIC
T_j = 125 °C



SURGE CHARACTERISTIC
T_j = 125 °C



TRANSIENT THERMAL IMPEDANCE
DOUBLE SIDE COOLED



Cathode terminal type DIN 46244 - A 4.8 - 0.8

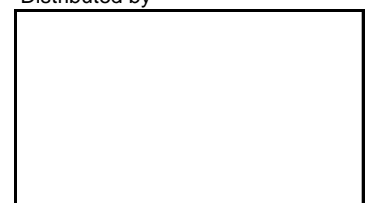
Gate terminal type AMP 60598 - 1

All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 μm.

In the interest of product improvement POSEICO SpA reserves the right to change any data given in this data sheet at any time without previous notice.

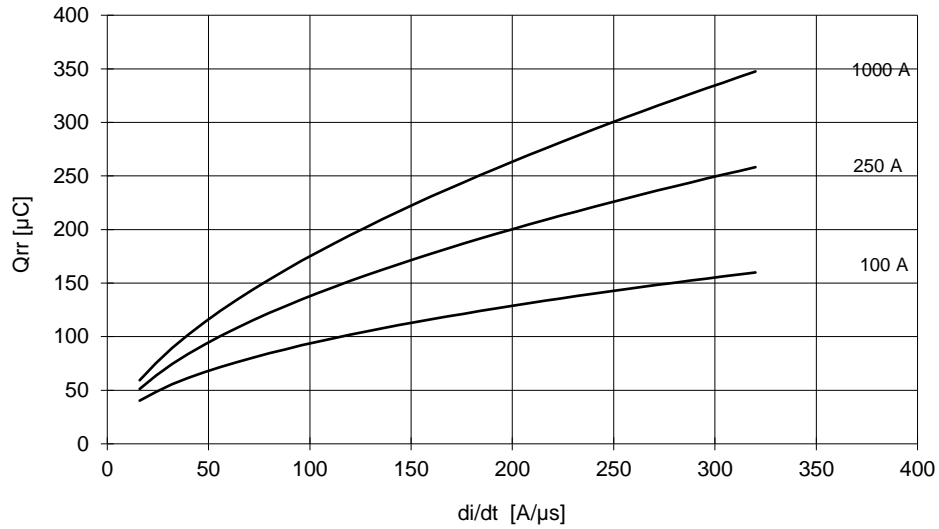
If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.

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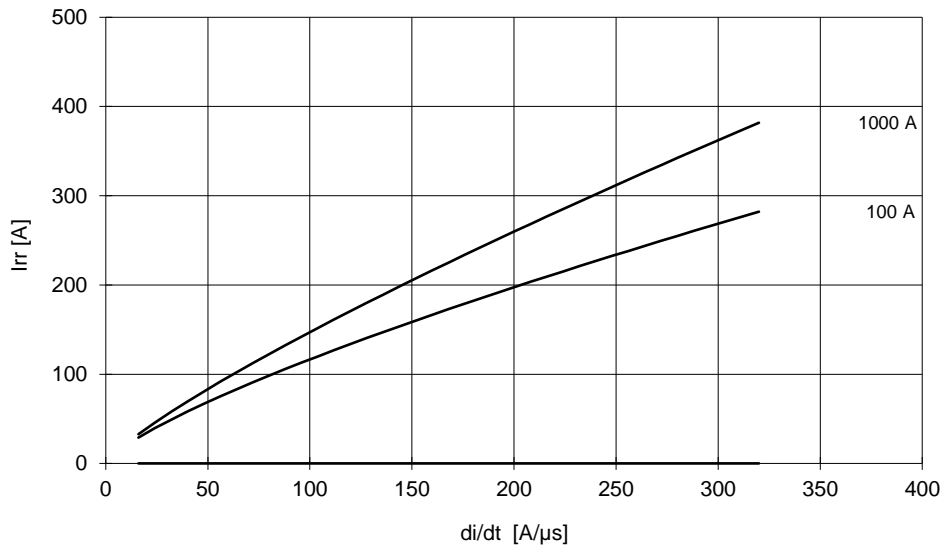


SWITCHING CHARACTERISTICS

REVERSE RECOVERY CHARGE
 $T_j = 125^\circ\text{C}$



REVERSE RECOVERY CURRENT
 $T_j = 125^\circ\text{C}$



$$t_a = I_{rr} / (di/dt) \quad t_b = t_{rr} - t_a$$

$$\text{Softness (s factor)} \quad s = t_b / t_a$$

$$\text{Energy dissipation during recovery } E_r = V_r \cdot (Q_{rr} - I_{rr} \cdot t_a / 2)$$

